Claims

1. A semiconductor wafer comprising a support substrate and a component substrate carried on the support substrate, the component substrate comprising:

a membrane layer having a plurality of spaced apart micro-machined components formed therein, and

a handle layer supporting the membrane layer and having a plurality of cavities corresponding to the micro-machined components extending through the handle layer to the respective corresponding micro-machined components,

the support substrate having a first surface facing in a first direction and defining a second surface facing in a second direction away from and opposite to the first direction, the support substrate defining an intermediate surface at a level intermediate the first and second surfaces and facing in the second direction, the support substrate comprising:

a plurality of spaced apart pedestals extending in the second direction from the intermediate surface into respective corresponding ones of the cavities in the handle layer of the component substrate, each pedestal terminating in the second surface spaced apart from the corresponding micro-machined component for accommodating movement of the micro-machined component,

at least one electrode carried on the second surface of each pedestal for co-operating with the corresponding micro-machined component,

a plurality of electrically conductive addressing tracks on one of the first and the intermediate surfaces of the support substrate for carrying address signals to be conducted to the respective electrodes, and

an electrical conductor corresponding to each electrode extending through a corresponding via through the corresponding pedestal from the electrode to a corresponding one of the addressing tracks on the support substrate for conducting the corresponding address signal to the corresponding electrode.

2. A semiconductor wafer as claimed in Claim 1 in which a plurality of mutually insulated electrodes are carried on each pedestal, and each electrode is connected to the corresponding one of the addressing tracks on the support substrate by the corresponding one of the electrical conductors extending through the corresponding

one of the vias.

3. A semiconductor wafer as claimed in Claim 1 in which the addressing tracks on the support substrate communicate the corresponding electrodes on the pedestals with a plurality of corresponding mutually insulated addressing terminals for addressing the electrodes.

4. A semiconductor wafer as claimed in Claim 3 in which the support substrate comprises a terminal carrier extending in the second direction from the intermediate surface for carrying the addressing terminals, and an electrical conductor corresponding to each addressing terminal extends from the corresponding addressing terminal through a corresponding via through the terminal carrier to the corresponding one of the addressing tracks on the support substrate for communicating the addressing terminal with the corresponding addressing track.

5. A semiconductor wafer as claimed in Claim 4 in which the terminal carrier terminates in the second surface, and the addressing terminals are located on the second surface.

6. A semiconductor wafer as claimed in Claim 1 in which the addressing tracks are located on the first surface of the support substrate.

7. A semiconductor wafer as claimed in Claim 6 in which the vias through the respective pedestals extend to the first surface for accommodating the corresponding electrical conductors therethrough to the addressing tracks.

8. A semiconductor wafer as claimed in Claim 1 in which the addressing tracks are located on the intermediate surface of the support substrate, and the vias through the respective pedestals extend to the intermediate surface for accommodating the corresponding electrical conductors to the addressing tracks.

9. A semiconductor wafer as claimed in Claim 1 in which the handle layer

defines a first surface of the component substrate, the first surface of the component substrate facing in the first direction, and the component substrate being carried on the support substrate with the first surface of the component substrate abutting the intermediate surface of the support substrate.

10. A semiconductor wafer as claimed in Claim 1 in which the support substrate comprises a base layer defining the first and the intermediate surfaces, the pedestals extending in the second direction from the base layer.

11. A semiconductor wafer as claimed in Claim 10 in which an insulating layer is located between the base layer and the respective pedestals of the support substrate.

12. A semiconductor wafer as claimed in Claim 11 in which the insulating layer extends over the surface of the base layer of the support substrate and defines the intermediate surface.

13. A semiconductor wafer as claimed in Claim 1 in which the transverse cross-sectional area of each pedestal is substantially similar to the area of the corresponding micro-machined component in plan view.

14. A semiconductor wafer as claimed in Claim 1 in which the transverse cross-sectional area of each cavity in the handle layer of the component substrate substantially defines the transverse cross-sectional area of the corresponding pedestal.

15. A semiconductor wafer as claimed in Claim 1 in which the respective pedestals are identical to each other.

16. A semiconductor wafer as claimed in Claim 1 in which the second surfaces of the respective pedestals define a common plane.

17. A semiconductor wafer as claimed in Claim 5 in which the second surface defined by the terminal carrier defines a common plane with the second surfaces of the respective pedestals.

18. A semiconductor wafer as claimed in Claim 1 in which an insulating layer is located between the handle layer and the membrane layer of the component substrate.

19. A semiconductor wafer as claimed in Claim 18 in which each cavity through the handle layer of the component substrate extends through the insulating layer between the handle layer and the membrane layer to the corresponding micro-machined component.

20. A semiconductor wafer as claimed in Claim 1 in which the membrane layer and the handle layer of the component substrate are of semiconductor material.

21. A semiconductor wafer as claimed in Claim 1 in which the support substrate is of semiconductor material.

22. A semiconductor wafer as claimed in Claim 1 in which the micro-machined components are micro-mirrors.

23. A semiconductor wafer as claimed in Claim 1 in which the respective micro-machined components are identical to each other.

24. A semiconductor wafer as claimed in Claim 1 in which the micro-machined components are arranged in a matrix array defining a plurality of spaced apart columns and spaced apart rows of the micro-machined components.